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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,315	04/08/2004	Andrei Grebennikov	18154	7461

26794 7590 03/10/2006

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EXAMINER	
NGUYEN, HIEU P	
ART UNIT	**PAPER NUMBER**
2817	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

N/A

Office Action Summary	Application No.	Applicant(s)	
	10/820,315	GREBENNIKOV ET AL.	
	Examiner	Art Unit	
	Hieu P. Nguyen	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim objections

Claims 6-7 are objected to because of the following informalities:

Claim 6, line 8, "a DC reference current" should correctly be -- a DC reference voltage --.

Claim 7, lines 2-3, "a DC reference current" should correctly be -- a DC reference voltage --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamamoto (US 6043714).

Regarding claims 1 and 6, Fig. 1 of Yamamoto discloses a method as well as a structure for bias a power amplifier (similar to Applicant's Fig. 4) comprising: a first transistor (Tr1) with a reference voltage (Vref) coupled **directly** to its base terminal; a second transistor (Tr2) coupled to the emitter terminal of the first transistor at its collector terminal; and a third transistor (TrA) with its base terminal coupled to the first and second transistors, and to an input signal, **meeting claims 1 and 6.** In addition, Yamamoto discloses the input signal comprises a radiofrequency signal (see Fig. 4, RFin), **meeting claim 3.**

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Apel (U.S. 6894561).

Regarding claims 1-6, Fig. 4 of Apel discloses a method as well as a structure for bias a power amplifier (similar to Applicant's Fig. 4) comprising: a first transistor (426) with a reference voltage (a voltage dropped across the resistor (434) can be read as the reference voltage) coupled directly to its base terminal; a second transistor (427) coupled to the emitter terminal of the first transistor at its collector terminal; and a third transistor (428) with its base terminal coupled to the first and second transistors, and to an input signal (RFin), thus **meeting claims 1 and 6** as expected. In addition, Apel discloses a resistor (see Fig. 4, resistor 435) coupled in series between the emitter terminal of the first transistor and the collector terminal of the second transistor, **meeting claim 2**. In addition, Apel further discloses the input signal comprises a radiofrequency signal (see Fig. 4, RFin), **meeting claim 3**. In addition, Apel discloses the bias circuit, wherein a second reference voltage applied to the base of the third transistor is implicitly linear [col. 3, lines 15-19], **meeting claim 4**. In addition, Apel discloses the bias circuit, wherein the quiescent current of the bias circuit is implicitly linear (col. 3, lines 15-19), **meeting claim 5**.

Claim 7-8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Apel in view of Nishimura (US 6809592).

Regarding claim 7, Apel discloses everything claimed as applied to claim 6 except for a method for biasing a power amplifier "wherein the step of applying a DC reference current comprises applying a current in the range from 10 to 100 microamperes". However, Nishimura [col. 3, lines 51-58] disclose a method for biasing a power amplifier, wherein the steps of applying a DC reference current comprises applying a current in the range of about tens of micro microamperes.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Nishimura into the power amplifier of Apel by "applying a DC reference current in the range from tens of microamperes". The ordinary artisan would have been motivated to modify Apel in the manner set forth above for at least the purpose of minimizing power consumption [Nishimura: col. 2, lines 22-25], **meeting claim 7**. In addition, Apel discloses the method a reference voltage applied to the at least one device cell is implicitly linear [col. 3, lines 15-19], **meeting claim 8** as well.

Claim 9-10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art view of Apel (US 6894561).

Regarding claim 9, Applicant's prior art (Fig. 1) shows a power amplifier circuit comprising: at least one control circuit (110) coupled to an input terminal (101);
a power amplifier array (120) coupled to the at least one control circuit; and
an adder (140) coupled to at least one output of the power amplifier array and coupled to an output terminal (102). Applicant's prior art fails to show "the power amplifier array further

comprises at least one bias circuit". However, Fig. 4 of Apel discloses a power amplifier (similar to Applicant's Fig. 4) comprising: a first transistor (426) with a reference voltage (Vbias1) coupled to its base terminal; a second transistor (427) coupled to the emitter terminal of the first transistor at its collector terminal; and a third transistor (428) with its base terminal coupled to the first and second transistors, and to an input signal (RFin).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Apel into the power amplifier of Applicant's prior art by having the specific bias circuit. The ordinary artisan would have been motivated to modify Applicant's prior art in the manner set forth above for at least the purpose of maintaining linearity of the power amplifier [Apel: col. 2, lines 6-9], **meeting claim 9**.

Regarding claim 10, Applicant's prior art discloses everything claimed as applied to claim 9 except for "the power amplifier, wherein a second reference voltage applied to the base of the third transistor is substantially linear. However, Apel discloses [col. 3, lines 15-19] the power amplifier, wherein a second reference voltage applied to the base of the third transistor is substantially linear.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Apel into the power amplifier of Applicant's prior art by having a second reference voltage linearly applied to the base of the third transistor. The ordinary artisan would have been motivated to modify Applicant's prior art in the manner set forth above for at least the purpose of maintaining linearity of the power amplifier [Apel: col. 2, lines 6-9], **meeting claim 10**.

Response to Arguments

Applicant's arguments filed 01/17/2006 have been fully considered but they are not persuasive.

Regarding claims 1 and 6, a voltage dropped across the resistor (434) can be considered as the reference voltage that is coupled directly to the first transistor's base, thus meeting the claimed language of "a first transistor with a reference voltage coupled directly to its base terminal" (note: even a reference voltage **source** couples directly to the first transistor's base is functional equivalent to a reference voltage couples directly to the first transistor's base).

Regarding claims 9 and 10, Apel doesn't suggest using the circuit with the conventional amplifier array circuit. However it would have been obvious to incorporate his teaching into the power amplifier of Applicant's admitted prior for at least the purposes mentioned in claims 9 and 10, since Applicant's admitted prior art shows the conventional amplifier array circuit that doesn't required any specific bias circuit, thus Apel's circuit can be implemented into the Applicant's admitted prior art one.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hieu Nguyen whose telephone number is 571-272-8577. The examiner can normally be reached on M-F 8-5.

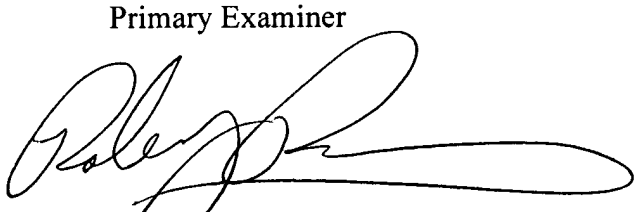
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 517-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hieu Nguyen
AU: 2817

hn

Robert Pascal
Primary Examiner



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